

Symbolic Analysis And Reduction Of VLSI Circuits
By Zhanhai Qin

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Dimensionality reduction of symbolic data should find applications in The authors expect that this will be a new direction in symbolic data analysis, <http://www.sciencedirect.com/science/article/pii/016786559400085H>

Symbolic analysis is an intriguing topic in VLSI designs. The analysis methods are crucial for the applications to the parasitic reduction and analog circuit evaluation. <http://mikesoft06.blogspot.com/>

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Symbolic Analysis and Reduction of VLSI Circuits Qin Zhanhai, Qin J., For analog circuit designs, symbolic analysis provides the relation between the tunable

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reduction, static analysis and symbolic reasoning support. Since these issues are harbingers of those being faced in multicore programming, the

<http://formalverification.cs.utah.edu/pdf/vmcai-mpi.pdf>

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<http://discover.tudelft.nl:8888/recordview/view?recordId=aleph%3A000354388&language=en>

Symbolic circuit analysis is a formal technique of circuit analysis to calculate the behaviour or characteristic of an electric/electronic circuit with the

http://en.wikipedia.org/wiki/Symbolic_Circuit_Analysis

Using Sensitivities for Symbolic Analysis and Model Order Reduction of Systems with Parameter Variation

http://link.springer.com/chapter/10.1007/978-3-642-25100-9_22

Sheldon Tan's publication list. Symbolic Analysis and Reduction of VLSI Circuits, Springer Publisher, 2005, ISBN: 0-387-23904-9; e-ISBN: 0-387-23905-7.

http://www.academia.edu/4553924/Sheldon_Tans_publication_list

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Reduction of design complexity especially for the extracted high-order RLCM networks is crucial for The idea is to perform the hierarchical symbolic analysis

http://www.ece.ucr.edu/~stan/project/vsclab_wiki/index.php/Compact_Modeling,_Reduction_and_Simulation_of_Interconnect_Parasitic_Circuits

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Analysis, reduction and avoidance of crosstalk on VLSI Zhanhai Qin, such as model order reduction in the design and analysis of VLSI circuits.

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Fast and robust symbolic model order reduction with analog insydes. Nowadays analog circuits become more and more complex. The growing number of devices hinder to

<http://www.swmath.org/software/10185>

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Fractal symbolic analysis compares a program and its transformed version by repeatedly simplifying these we propose memory reduction as a new approach to data
<http://dl.acm.org/citation.cfm?id=377792.377804>

To avoid scalability issues associated with symbolic analysis, many test-suite reduction techniques, based on different measures of redundancy,
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